Bandgap Voltage Reference – Simulations in Cadence and Layout Design

Rumiana Iliyanova Todorova, Tihomir Borisov Takov and Atanas Stoyanov Pangev

Abstract – **Analog and digital circuit ultimately need a voltage reference. The reference establishes a state point used by other subcircuits to generate predicable results. This reference point should not fluctuate significantly under various operating conditions such as moving power supply voltage, temperature variation, and transient loading events. A example a circuit amplification where reference are intrinsically require are linear regulators. A bandgap reference circuit for 0.35 µm CMOS technology operates in an essentially temperature independent manner and having low supply voltages. In the conventional bandgap circuit, the output voltage V_{REF} is the sum of built-in voltage of the diode V_{BE} and thermal voltage V_T. Therefore V_{REF} is about 1.2 V that is passing to regulator, which limits a low supply by linear regulator operation below 3.2 V.**

Keywords – **Bandgap Voltage Reference, Cadence, Matching**

I. Introduction

Bandgap reference voltages have been developed to provide a stable voltage supply that is insensitive to temperature variations over a wide temperature range. These circuits operate on the principle of compensating the negative temperature drift of a bipolar transistor's base-emitter voltage (VBE) with the positive temperature coefficient of the thermal voltage VT. A known negative temperature drift due to VBE is first generated. A positive temperature drift due to the thermal voltage is then produced, and is scaled and subtracted from negative temperature drift to obtain a nominally zero temperature dependence.

The basic scheme of Bandgap is presented on Figure 1.

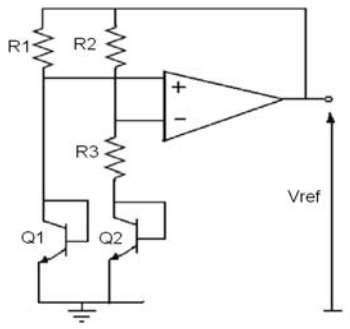

Figure 1. Principle scheme of bandgap.

R. Todorova and T. Takov are with the Department of Microelectronics, Technical University of Sofia, 8 Kliment Ohridski St., 1797 Sofia, Bulgaria, e-mail: takov@ecad.tu-sofia.bg, rumito.todorova@gmail.com

A. Pangev is with Melexis Bulgaria, 2 Samokovsko Shose Str., 1138 Sofia, Bulgaria, e-mail: apn@melexis.com

The circuit is contented to amplifier, two bipolar transistors Q1 and Q2 (connect as diodes) with equal emitters areas and resistors. The amplifiers have a large coefficient of amplifier so that the potentials of two his inputs are equal:

$$R1.I_{R1} \approx R2.I_{R2} \tag{1}$$

$$I_{R1} = \frac{V_T}{R}\ln\left(\frac{I_{R1}}{I_{R2}}.\frac{A1}{A2}\right) = \frac{V_T}{R}\ln\left(\frac{R1}{R2}\right) \tag{2}$$

VREF is calculated with formula:

$$V_{REF} = V_{BE1} + R1.I_{R1} = V_{BE1} + \frac{R1}{R3}\varphi_T \ln\left(\frac{R1}{R2}\right) \tag{3}$$

II. Bandgap Voltage Reference

In Figure 2 is shown a voltage reference with supply 3.1 V. The basic blocks of scheme are explained below. Transistors M2 and M4 are a differential pair of differential amplifier. Their gates are connected to resistors R1, R2, R3 and bipolar transistors Q1 and Q2. These elements are the main part from the voltage reference circuit. Transistors M1 and M3 are a current mirror in the differential amplifier and M10a and M10b are connected in series forming a current generator. The resistors R4a, R4b, R4c and R4d are connected each other. M5 and M12 are connected in common-source to increase the voltage gain. The transistors M7 and M1 are connected to common-drain to make faster the start up of the circuits and to ensure an output resistance. The amplifier has a tree-stage configuration. The first stage is a differential amplifier, the second stage is a common gate and third stage is a common drain.

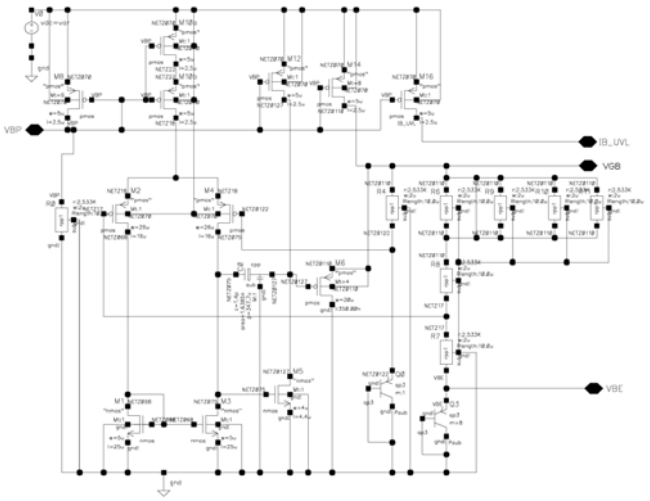

Figure 2. Bandgap voltage reference

A. Common-drain Stage

In electronics, a common-drain amplifier, also known as a source follower, is one of three basic single-stage field effect transistor (FET) amplifier topologies, typically used as a voltage buffer. In this circuit the gate terminal of the transistor serves as the input, the source is the output, and the drain is common to both (input and output), hence its name. The analogous bipolar junction transistor circuit is the common-collector amplifier.

B. Common-source Stage

A common-source amplifier is typically used as a voltage or transconductance amplifier. The easiest way to tell if a FET is common source, common drain, or common gate is to examine where the signal enters, and leaves. The remaining terminal is what is known as "common". In this example, the signal enters the gate, and exits the drain. The only terminal remaining is the source. This is a common-source FET circuit. The analogous bipolar junction transistor circuit is the common-emitter amplifier.

C. Differential Amplifier

A differential amplifier is a type of electronic amplifier that multiplies the difference between two inputs by some constant factor (the differential gain). Many electronic devices use differential amplifiers internally. Given two inputs V_{IN}^{+} and V_{IN}^{-}, a practical differential amplifier gives an output Vout:

$$V_{out} = A_D\left(V_{IN}^{+} - V_{IN}^{-}\right) + A_C\left(\frac{V_{IN}^{+} + V_{IN}^{-}}{2}\right), \qquad (4)$$

where Ad is the differential-mode gain and Ac is the common-mode gain.

The common-mode rejection ratio is usually defined as the ratio between differential-mode gain and common-mode gain:

$$CMRR \cong \frac{A_D}{A_C} \qquad (5)$$

In the above equation, as Ac approaches zero, CMRR approaches infinity. Thus, for a perfectly symmetrical differential amplifier with Ac = 0, the output voltage is given by:

$$V_{out} = A_D\left(V_{IN}^{+} - V_{IN}^{-}\right) \qquad (6)$$

Note that a differential amplifier is a more general form of amplifier than one with a single input; by grounding one input of a differential amplifier, a single-ended amplifier results.

III. Simulations in Cadence

A. DC Analysis Stability over Temperature

The first and most important simulation in Cadence is DC verse temperature in range from -40˚C to 120˚C. This analysis determines the correct operation of the scheme. The voltage in room temperature is 1.207 V and that is showed in Figure 3.

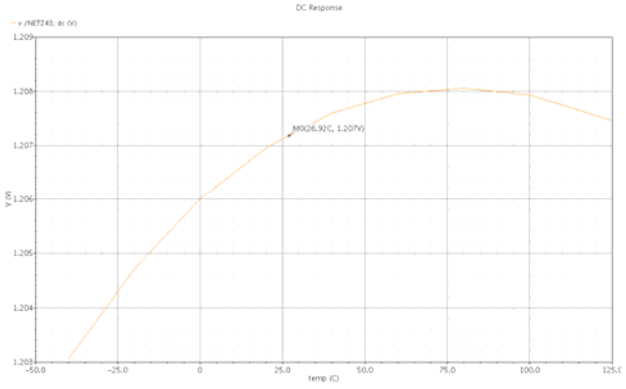

Figure 3. DC analysis stability over temperature.

B. Transient Analysis Stability over Output Voltage

On the output of bandgap are connected impulse source ipwl. On Figure 4 is shown the voltage of the impulse source and the current through him.

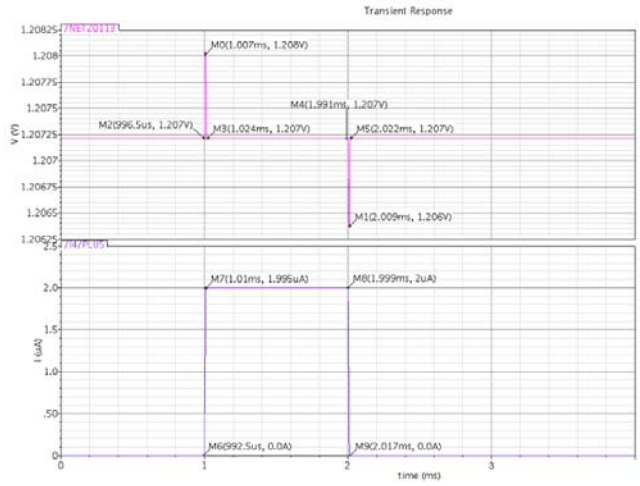

Figure 4. Transient analysis stability over output voltage

The results of the analysis are showing that the voltage through source increase with several milivolts and after that establish its state. At the same time the positive front of current increase. At the negative front of current the result is the same but the voltage decrease and return to normal work. The increase and decrease of voltage is in permissible borders.

C. Simulation of the Amplifier

Figure 5 shows amplitude-frequency and the phase-frequency characteristics. From the graph of magnitude response is determined gain voltage Au=107.8 dB, transit frequency f_T=0,9 kHz and bandwidth frequency $f_{(-3dB)}$=4.104 Hz. From the graph of phase frequency response is defined phase magnitude - 57 deg where the negative feedback didn't change and ensured the stability of the scheme.

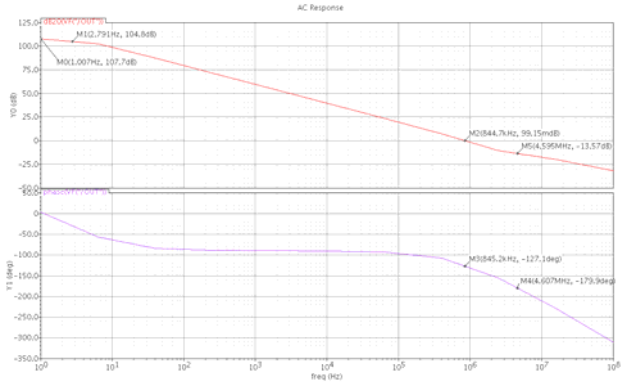

Figure 5. Amplitude-frequency and the phase-frequency characteristics

D. Simulation of the Start-up Time

On the input of scheme is placed impulse source on voltage with following adjustment:

TABLE 2. VPWL WITH FOLLOWING ADJUSTMENT

Time, ms	0	1
Voltage, V	0	3.1

Transient analysis is simulated with at different temperature. The measuring is made on the output of scheme. The engraving is showed on Figure 6. The time of establish decrease with increase of temperature. At room temperature 27 ˚C the time is biggest 2.5 μs and the time corresponding on require value.

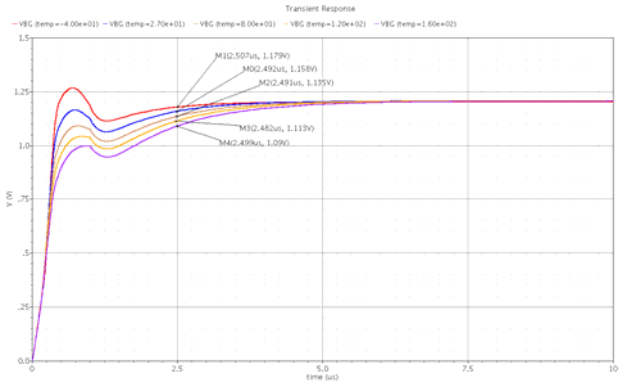

Figure 6. Engraving on stabilize the time of establish.

E. Simulation of the Maximum Supply Current in Worse Cause

Together with DC analysis is permit Corner analysis. The current of input of bandgap is showed on Figure 7. It can seen, that the input current is 116 μA.

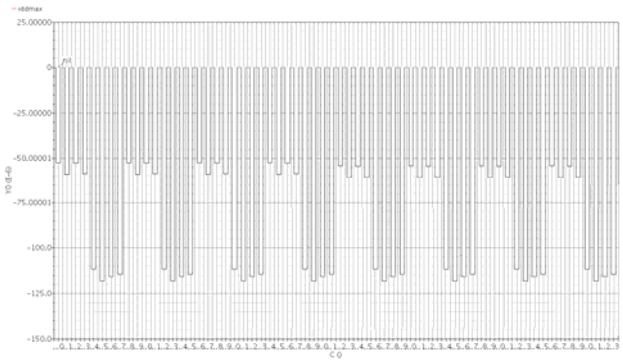

Figure 7. Engraving for maximum of supply current

IV. LAYOUT AND MATCHING OF BANDGAP

A. Matching

Basic idea of matching: if you have a collection of nominally identical devices and you did everything right in laying them out, they will have a β (current) and a VT (threshold voltage) mismatch, described with the so called standard deviation σ:

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{A_\beta^2}{W.L} + S_\beta^2 D^2 \qquad (7)$$

$$\sigma^2(V_T)\frac{A_{Vt}^2}{WL} + S_{Vt}^2 D^2 , \qquad (8)$$

where Aβ, AVt, Sβ and SVt are technology dependent constants and D is the separation between the devices. The second term in the equation is typically not significant except over very distances and for large transistors. The key idea is the square-root dependence of the standard deviation of mismatch factors with respect to the area of the device. In two words, two devices are matched better if they are layed out at a near distance, have large dimensions and their surrounding are equal. For example Figure 8.

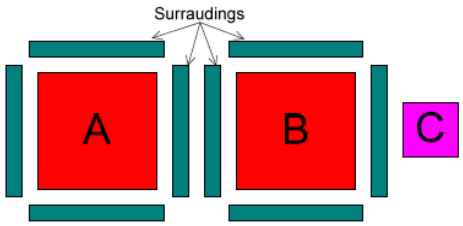

Figure 8. The basic idea of matching.

B. Transistors' Matching

- Only try to match device of equal nature. Do not match MOS transistors with bipolar, nor diffused resistor with polysilicon ones, etc;
- Increase the size of the device for better current matching;
- Lay out the device at minimum distance from each other;
- Lay out devices with the same orientation with respect to the silicon crystal putting them in parallel. MOS transistors

that are not oriented in the same way cause different carrier mobility's and current directions in the crystal;

C. Current Mirror Layout

- Use the same and large L – for small L the effect of λ (channel length modulation) – is stronger;
- All devices to be matched must have the same area to perimeter ratio. In this way, they have the same ratio of global to local errors, which optimizes matching. For example, a current mirror with a ratio of two is better to take two times the same transistors than to take a single transistor with double W.
- Use the same W and L, and vary M
- It is wrong, if the matched current mirror transistors are crossed indiscriminately by any wires

The better matching of mirror current is presented on Figure 9.

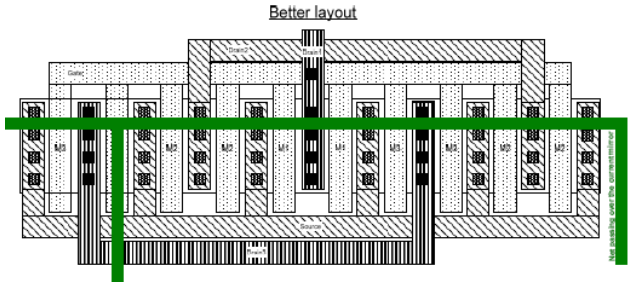

Figure 9. Better layout of mirror current.

D. Differential Pair Transistors Layout

- The differential stage us a typical bridge circuit, i.e. it's vary sensitive to any mismatching;
- The differential pair transistors should have large W and L for smaller edge effects;
- The differential pair transistors should have large W so as to achieve a small input offset voltage;
- For large transistors symmetry becomes more difficult to establish. Thus, the input transistors M1 and M2 should be divided into two or more parts.

E. Resistors Matching

Matching single resistor is senseless although in some cases it is reasonable to draw it not as meander, but to divide it into certain amount of equal parts (primitives). Thus with only one mask change (for example Metal1 mask) it is possible to the change the resistor value.

This way of laying out is sometimes used for large resistors value. From the viewpoint of matching and reproducibility, this structure is preferable to serpentine topologies, where the corners contribute significant resistance.

If we have many geometrically equal resistors, placed in row, the absolute value of each of them will be different due tp the different gradients (implantation, temperature…)

The most common solution for matching is "centroid" technique. The idea is that every single resistor from the schematic should be represented by at least 2 different primitives, placed indifferent areas at the wafer – so their common values will be compensated by gradient of the mismatching cause. Therefore sequential resistors should be at equal distance away from imaginary axis of symmetry, which separates layout resistors into two equal parts.

G. Layout of Bandgap Voltage Reference

I use the rules about matching described above for transistors, mirror currents, differential pair and resistors to match the scheme of voltage reference. The layout is presented on Figure 10. The scheme is verified with DRC (design rule check) and LVC used to extract devices and nets from a layout, and then compare the extracted layout netlist to a schematic netlist.

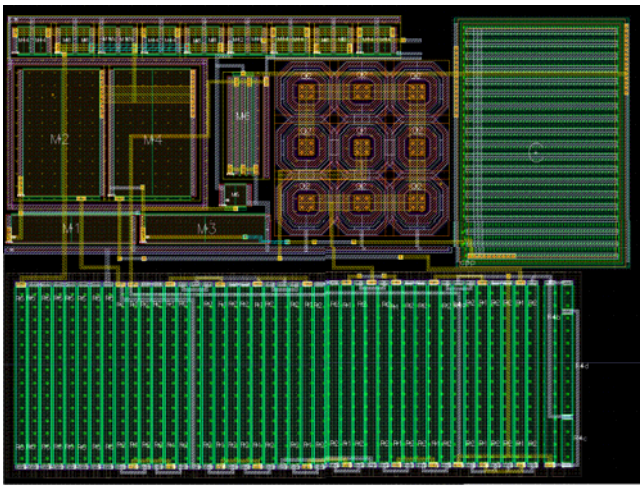

Figure 10. Voltage reference layout.

V. Conclusion

The simulation results show that the proposed bandgap has an excellent performance. It has output voltage independent of temperature with a typical value of 1.2 V. The amplifier has a high gain voltage. It created a layout of scheme conformable to the rules of matching. Then checked a design rules and are extracted a parasitic element of the topography. It can be concluded that the extracted parasitic elements do not substantially affect the work of the scheme and introduced many small changes in the values of the output voltage.

VI. Acknowledgement

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